REMARKS

By the above amendments the specification was amended to update the status of the parent application referred to on page 1 of the specification. Claim 1 has also been amended to correct a redundancy in line 10 of the claim. Thus, claims 1-10 remain in the application.

Claims 1-13 were provisionally rejected in the outstanding Office Action under the judicially created doctrine of obviousness type double patenting over claims 1-6 of co-pending, commonly owned application no. 10/821,842, as indicated on page 2 of the Office Action. Responsive to this provisional rejection, enclosed herewith is a Terminal Disclaimer on behalf of the assignee of the both applications, Hitachi, Ltd., disclaiming the term of the patent issuing on the subject application which would extend beyond the full statutory term of any patent issuing on their commonly owned application no. 10/821,842. In view of the submission of the Terminal Disclaimer, reconsideration and withdrawal of the provisional rejection is requested.

Claims 1-13 were further rejected in the outstanding Office Action under 35 U.S.C. §102(e) as being anticipated by the patent to Soininen et al., U.S. Patent No. 6,482,740. The patent to Soininen et al. was cited for the reasons and in the manner stated on pages 3-6 of the Office Action. This rejection is hereby traversed and reconsideration thereof is respectfully requested in view of Applicants remarks as set forth below.

The present invention recited in the application claims is for a process for manufacturing a semiconductor integrated circuit device. Each of the independent claims 1, 5 and 8 of the application claims recites a process involving steps (a), (b), (c) and (d) as generally referred to below. See

Figures 9, 12, and 15 with respect to an example embodiment, which is referred to.

(a) forming an insulating film (gate insulating film 9A) on a wafer (wafer 1) as described in the specification at page 6, line 22 to page 37, line 2, for example;

(b) forming a metal film (tungsten film 11A, for example) on the insulating film (9A), see page 40, line 10 through line 17 of the specification;

(c) heat treating the wafer (1) in a water-vapor-and hydrogen-containing gas atmosphere, see page 41, line 14 to page 42, line 21 of the specification, for example;

(d) patterning the metal film (9A) to form a metal gate electrode (gate electrode 11), see page 42, line 14 to line 17 of the specification, for example.

It is stated in the Office Action that the patent to Soininen et al. discloses Applicant's claimed process, particular reference being made to column 6, lines 55-67 of the patent. However, Applicants respectfully note that the process of their invention is not disclosed in Soininen et al., and particularly it is not disclosed in column 6, lines 55-67 of the patent which only generally refers to an atomic layer deposition (ALD) process.

In column 5, line 59 to column 6, line 7 and Figure 3 of Soininen et al., the structure of the MOS transistor is described. However, the process for the MOS transistor has not been described at all in Soininen et al. The reference does not disclose or suggest Applicants claimed process. In fact, the disclosed process in Soininen et al. relates to forming a metal oxide thin film preferably by atomic layer deposition (ALD) and subsequently reducing the metal oxide film in an ALD reactor using one or more vaporized organic

components that consist of at least one functional group selected from the group consisting of -OH, -CHO and -COOH. This is not the process of the present invention involving the aforementioned steps as specifically recited in each of the application claims wherein the wafer is heat treated in a water-vapor-and hydrogen-containing gas atmosphere having a water vapor-hydrogen partial pressure ratio set at a ratio permitting oxidation of silicon without substantial oxidation of the refractory metal formed over the insulating film.

In view of this, it is respectfully submitted that claims 1-13 are not anticipated by Soininen et al. under 35 U.S.C. §102(e). Accordingly, reconsideration and allowance of the claims is respectfully requested.

A Petition for Extension of Time to permit the timely filing of this Amendment and Terminal Disclaimer is being filed herewith.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (Case No. 501.38505CX2) and please credit any excess fees to such deposit account.

Respectfully submitted,

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RJS/kmh

Attachments